

Sirindhorn International Institute of Technology  
Thammasat University at Rangsit  
School of Information, Computer and Communication Technology

## ECS 371: Problem Set 6 Solution

**Semester/Year:** 1/2009

**Course Title:** Digital Circuits

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**Course Web Site:** <http://www.siiit.tu.ac.th/prapun/ecs371/>

**Due date: August 19, 2009 (Wednesday)**

### Instructions

1. The questions are assigned from the following textbook:

Thomas L. Floyd, [\*Digital Fundamentals\*](#), 10<sup>th</sup> Edition, Pearson Education International (2009).

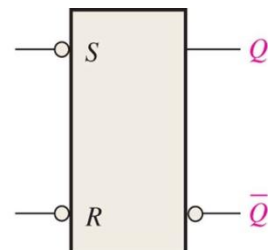
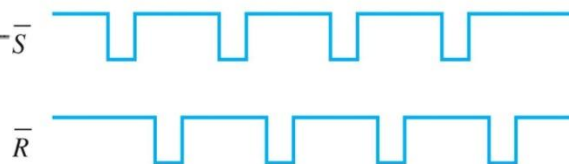
2. Only ONE of the problems will be graded. Of course, you do not know which problems will be selected; so you should work on all of them.
3. Late submission will not be accepted.
4. **Write down all the steps** that you have done to obtain your answers. You may not get full credit even when your answer is correct without showing how you get your answer.

### Chapter 7

- Please submit your solutions for the following questions: 2, 4, 8, 10, 12, 14, 18

1. If the waveforms in Figure 7-72 are applied to an active-LOW input S-R latch, draw the resulting  $Q$  output waveform in relation to the inputs. Assume that  $Q$  starts LOW.

► FIGURE 7-72

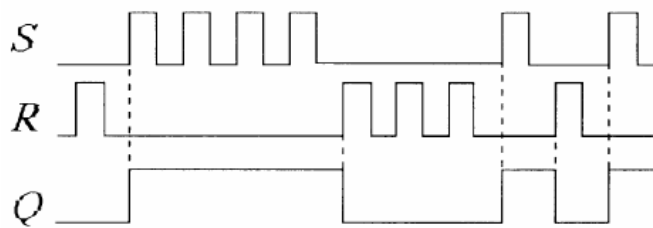


2. Solve Problem 1 for the input waveforms in Figure 7-73 applied to an active-HIGH S-R latch.

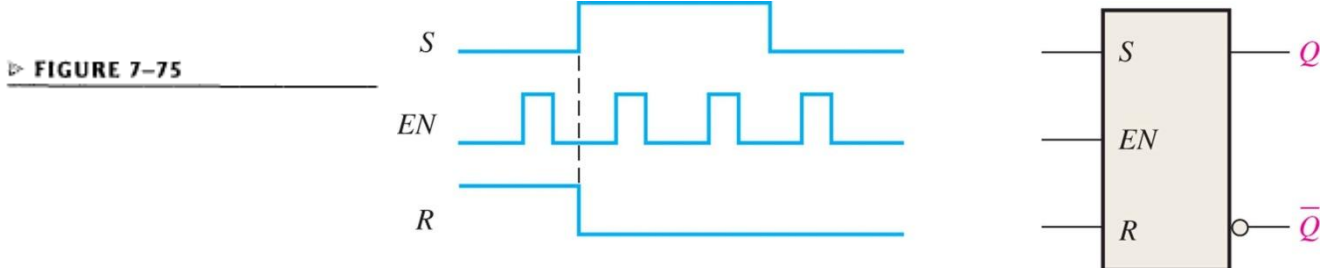


**Solution:**

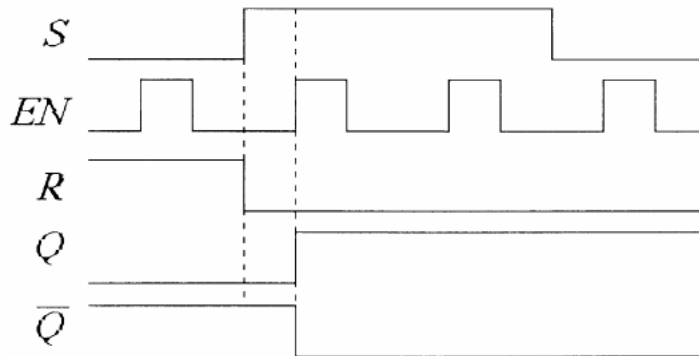
As in Problem 1, we assume that Q starts LOW.



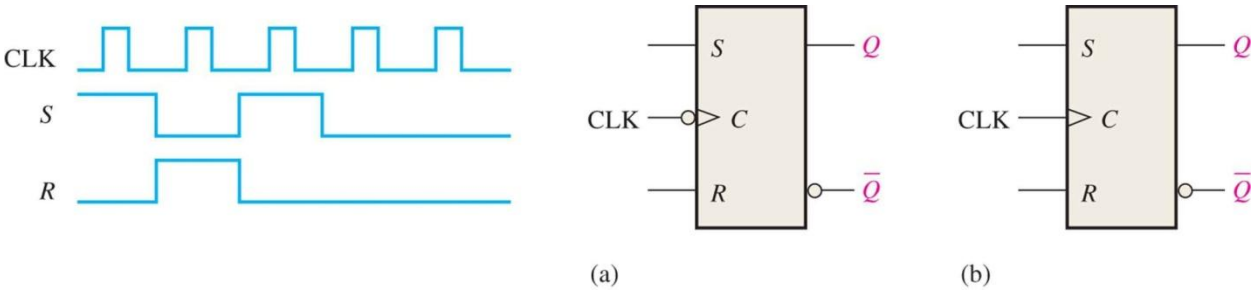
4. For a gated S-R latch, determine the  $Q$  and  $\bar{Q}$  outputs for the inputs in Figure 7-75. Show them in proper relation to the enable input. Assume that  $Q$  starts LOW.



**Solution:**

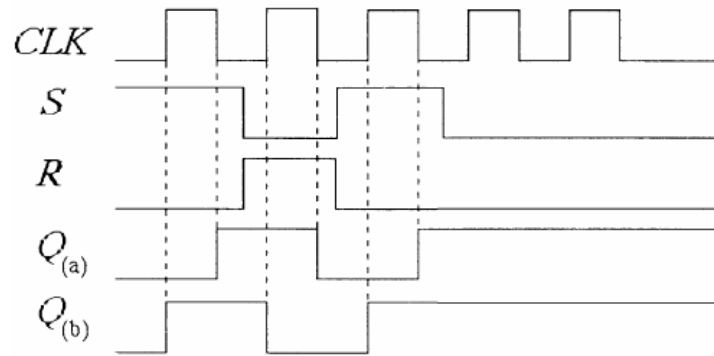


8. Two edge-triggered S-R flip-flops are shown in Figure 7-79. If the inputs are as shown, draw the  $Q$  output of each flip-flop relative to the clock, and explain the difference between the two. The flip-flops are initially RESET.



▲ FIGURE 7-79

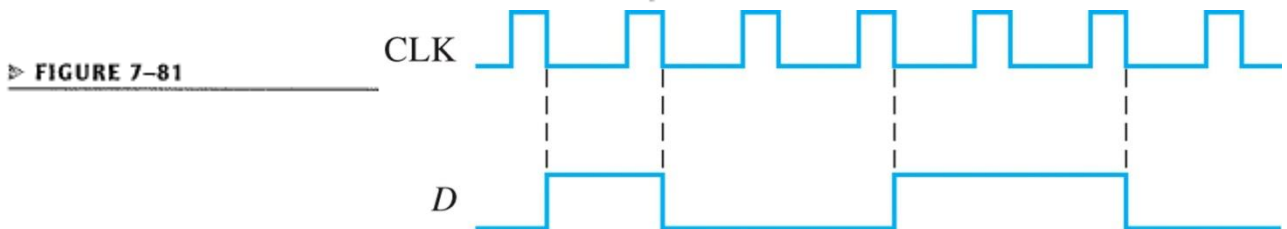
**Solution:**



- (a) The flip-flop triggers on the negative edge of the clock pulse.
- (b) The flip-flop triggers on the positive edge of the clock pulse.

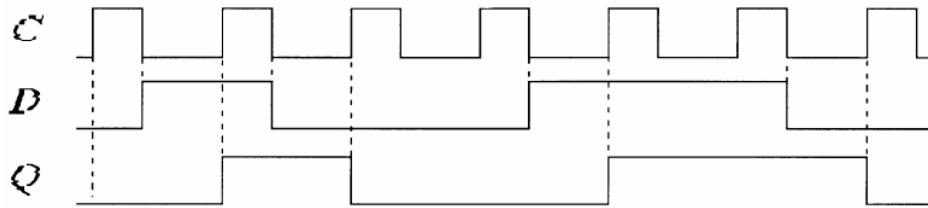
Notice that  $Q_a$  and  $Q_b$  are the same except that  $Q_a$  is half-cycle slower. For some S and R waveforms,  $Q_a$  and  $Q_b$  can be totally different.

10. Draw the  $Q$  output relative to the clock for a D flip-flop with the inputs as shown in Figure 7-81. Assume positive edge-triggering and  $Q$  initially LOW.



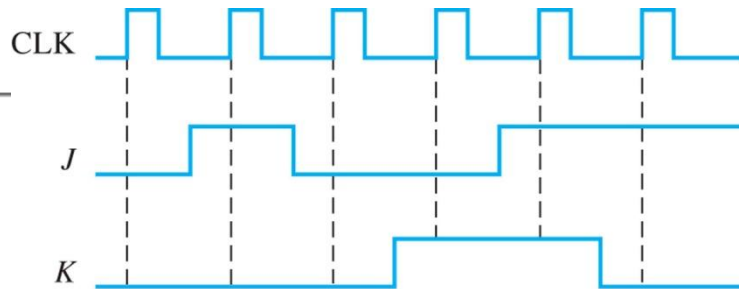
▶ FIGURE 7-81

**Solution:**

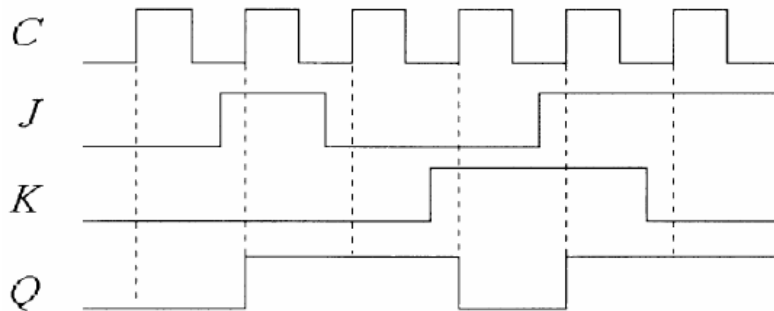


**12.** For a positive edge-triggered J-K flip-flop with inputs as shown in Figure 7-83, determine the  $Q$  output relative to the clock. Assume that  $Q$  starts LOW.

FIGURE 7-83

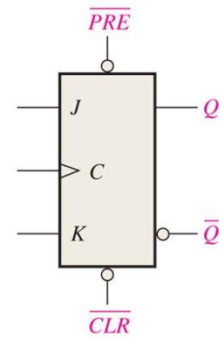
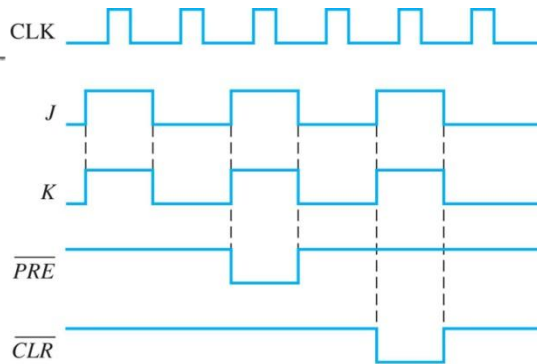


**Solution:**

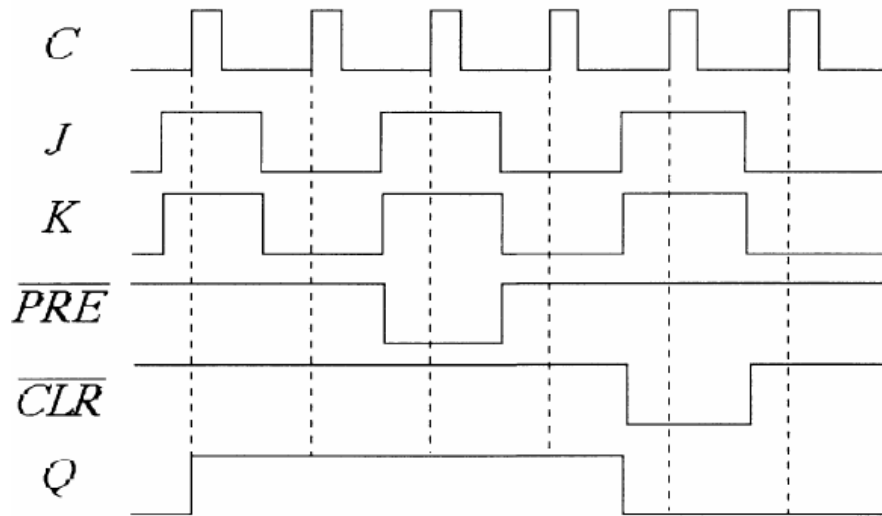


**14.** Determine the  $Q$  waveform relative to the clock if the signals shown in Figure 7-85 are applied to the inputs of the J-K flip-flop. Assume that  $Q$  is initially LOW.

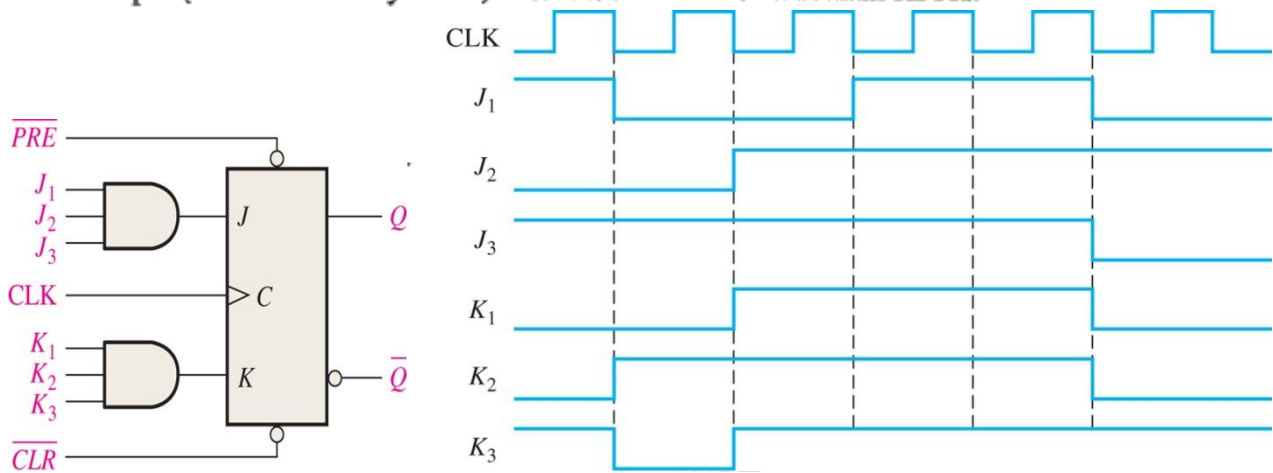
FIGURE 7-85



**Solution:**



**17.** For the circuit in Figure 7-87, complete the timing diagram in Figure 7-88 by showing the  $Q$  output (which is initially LOW). Assume  $\overline{PRE}$  and  $\overline{CLR}$  remain HIGH.

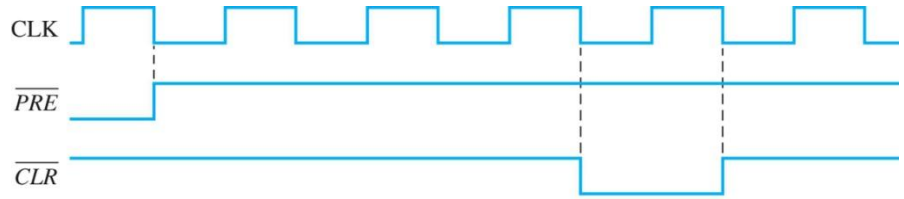


▲ FIGURE 7-87

▲ FIGURE 7-88

**18.** Solve Problem 17 with the same  $J$  and  $K$  inputs but with the  $\overline{PRE}$  and  $\overline{CLR}$  inputs as shown in Figure 7-89 in relation to the clock.

FIGURE 7-89



Solution:

